ABSTRACT OF THE DISCLOSURE

[1050] A PLL function may be implemented as a dual-loop structure having a first PLL circuit which generates an intermediate signal from the reference signal, and a second PLL circuit which generates an output signal from the intermediate signal. The intermediate signal frequency is preferably chosen at a value in which potential interference signals do not have much energy. The first loop preferably has low bandwidth to provide good input jitter attenuation, while second loop preferably has higher bandwidth to reduce phase noise of the output signal. The circuit preferably provides for a choice of several different intermediate frequencies to allow use where different intermediate frequencies may exist in each system. Moreover, in a system having two such dual-loop PLL circuits, each can be configured with a different intermediate frequency, so that interference from one to the other is reduced.